REMARKS

Claims 3-6, 9-12 and 15-25 are pending in the present application. Claims 3, 5, 9, 11 and 15 have been amended. Claims 18-25 have been presented herewith.

Finality of Office Action

The current Office Action dated November 26, 2003, has been made Final. The Examiner has asserted that Applicant's Amendment dated October 8, 2003, has necessitated the new grounds of rejection. Applicant respectfully disagrees for the following reasons.

Initially, Applicant respectfully submits that claims 3, 9 and 15 were each respectively amended in the Amendment dated October 8, 2003, to be in independent form responsive to the Examiner's acknowledgment of allowable subject matter in the previous Non-Final Office Action dated July 8, 2003. The other amendments to claims 3, 9 and 15 were merely for the purpose of improving form and antecedent, not to substantively change claim scope.

As set forth in Manual of Patent Examining Procedure section 706.07(a), "Under present practice, second or any subsequent actions on the merits shall be final **except** where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c)".

As further set forth in MPEP section 706.07(a), "A second or any subsequent

action on the merits in any application...should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed".

Clearly, the amendment of claims 3, 9 and 15 to respectively be in independent form should reasonably have been expected responsive to the Examiner's acknowledgment of allowable subject matter. Since claims 3, 9 and 15 were not amended to substantively change claim scope, the rejection of at least these claims based on prior art not previously of record, constitutes new grounds of rejection.

Accordingly, Applicant respectfully submits that the finality of the current Office Action dated November 26, 2003, is clearly improper, and should thus be withdrawn. **If the finality of the Office Action dated November 26, 2003, is to be maintained, the Examiner is respectfully requested to clearly establish on the record why the amendment of claims 3, 9 and 15 in the Amendment dated October 8, 2003, necessitated the new grounds of rejection, particularly in view of the above noted portions of MPEP section 706.07(a).**

Claim Rejections-35 U.S.C. 112

Claims 3, 5, 9 and 11 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

Claim 3 has been amended to feature in combination "forming a dielectric film on

the main surface", and "forming a conductive layer on the dielectric film". Claim 9 has been amended in a similar manner. Also, claim 5 has been amended to feature that "the gate electrode is formed so as to have a greater width at a bottom surface than at a top surface, after the implanting". Claim 11 has been amended in a similar manner. Applicant respectfully submits that claims 3, 5, 9 and 11 are in compliance with 35 U.S.C. 112, second paragraph, and thus respectively urges the Examiner to withdraw this rejection.

Claim Rejections-35 U.S.C. 102

Claims 3, 5, 6, 9, 11, 12, 15 and 17 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Hatano et al. publication: "A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance". This rejection is respectfully traversed for the following reasons.

The method of manufacturing a field effect transistor of claim 3 includes in combination "forming a gate electrode by etching the conductive layer using a mask formed thereon", "forming a source region and a drain region in the main surface", and "forming pocket regions in the semiconductor substrate by implanting ions using the mask, wherein the mask has a width less than a desired width necessary to define a gate length of the gate electrode, and the implanting is carried out from an upward direction of the mask to the semiconductor substrate using the mask". Applicant respectfully submits that the Hatano et al. publication as relied upon by the Examiner

does not disclose these features.

Particularly, the device structures in Figs. 1 and 2 of the Hatano et al. publication do not include a mask that has a width less than a desired width necessary to define a gate length of a gate electrode, as featured in claim 3. The Examiner has asserted that these features may be interpreted as realized in connection with step 3 (the third view in Fig. 2) of the Hatano et al. publication. However, Applicant respectfully submits that the Examiner has misinterpreted the Hatano et al. publication.

Particularly, the **mask** of claim 3 is featured as having a width less than a desired width necessary to define **a gate length** of the gate electrode.

The Examiner has interpreted the SiO_2 mask at the top of the structure in Fig. 1 of the Hatano et al. publication as the mask of claim 3. However, the SiO_2 mask in Fig. 1 of the Hatano et al. publicaton does not have a width less than a desired width necessary to define the gate length of the gate electrode, as featured in claim 3. That is, the gate length of the structure in the Hatano et al. publication should be considered as equivalent or corresponding to the horizontal length of the i-poly-Si region (white colored region) directly under the SiO_2 mask, as particularly illustrated in Fig. 1 and in the second and third views of Fig. 2. This i-poly-Si region is formed between the lightly-doped (LDD) n^- regions, and is essentially the channel region of the transistor structure. Accordingly, the width of the SiO_2 mask in Figs. 1 and 2 of the Hatano et al. publication is the same as the gate length of the transistor across the i-poly-Si region between the n^- LDD regions. The Hatano et al. publication therefore does not disclose or suggest a

mask having a width less than a desired width necessary to define a gate length of the gate electrode, as would be necessary to meet the features of claim 3.

To more clearly emphasize this point, enclosed as of interest is an excerpt from the Mead et al. textbook "Introduction to VLSI Systems". As illustrated in Fig. 1.3, gate length L is considered as a dimension of length of the region under the gate electrode between the source and drain diffusions, where no diffusion paths exist.

Consequently, it should thus be understood that the gate length in Figs. 1 and 2 of the Hatano et al. publication is equivalent or corresponds to the i-poly-Si region under the gate electrode between the n^- LDD regions, wherein no diffusion paths exist. The gate length in Figs. 1 and 2 of the Hatano et al. publication must therefore be interpreted as equal to the width of the SiO_2 mask. **Particularly, the poly-Si sidewalls in Fig. 1 of the Hatano et al. publication overlap the n^- LDD regions, and therefore do not contribute to gate length.**

Accordingly, Applicant respectfully submits that the method of manufacturing a field effect transistor of claim 3 distinguishes over the Hatano et al. publication as relied upon by the Examiner, and that this rejection of claims 3, 5 and 6 is improper for at least these reasons. If this rejection is to be maintained, the Examiner is respectfully requested to establish on the record how the width of the SiO_2 mask in Figs. 1 and 2 of the Hatano et al. publication may be interpreted as being less than a desired width necessary to define a gate length of the gate electrode.

The method of manufacturing a field effect transistor of claim 9 features in

combination that "the first mask has a width less than a desired width necessary to define a gate length of the gate electrode...". Applicant respectfully submits that the method of manufacturing a field effect transistor of claim 9 distinguishes over the Hatano et al. publication as relied upon by the Examiner for at least somewhat similar reasons as set forth above, and that this rejection of claims 9, 11 and 12 is improper for at least these reasons.

The method of manufacturing a field effect transistor of claim 15 includes in combination "implanting an impurity in a predetermined region in said semiconductor substrate under said conductive layer by an ion implantation using said etching mask as a mask, to form said pair of second impurity regions, wherein said etching mask has a width less than a desired width necessary to define a gate length of said gate electrode". As further featured, "said pair of second impurity regions being formed at an interval and having a conductivity type different than a conductivity type of said pair of first impurity regions".

As emphasized above, the Hatano et al. publication does not disclose an etching mask having a width less than a desired width necessary to define a gate length of a gate electrode. Moreover, the structure in the Hatano et al. publication includes n^- LDD regions and N+ source/drain regions of a same conductivity type. The Hatano et al. publication does not include a pair of second impurity regions having a conductivity type different than a conductivity type of a pair of first impurity regions that are a source and a drain. Accordingly, Applicant respectfully submits that a method of manufacturing a

field effect transistor of claim 15 distinguishes over the Hatano et al. publication as relied upon by the Examiner, and that this rejection of claims 15 and 17 is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 4, 10 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. However, Applicant respectfully submits that claims 4, 10 and 16 should be considered allowable by virtue of dependency upon independent claims 3, 9 and 15 respectively. Accordingly, amendment of claims 4, 10 and 16 to be in independent form is unnecessary.

Claims 18-25

Applicant respectfully submits that claims 18-22 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, at least by virtue of dependency upon independent claims 3, 9 and 15 respectively, and by further reason of the features therein. The Hatano et al. publication does not disclose forming pocket regions having a conductivity type opposite a conductivity type of source and drain regions, as featured in claims 18 and 20. Also, the Hatano et al. publication does not disclose forming pocket regions by implanting ions through a conductive layer into a semiconductor substrate, as featured in claims 19, 21 and 22.

The method of manufacturing a field effect transistor of claim 23 includes in combination "implanting ions through the conductive layer into the substrate under the etching mask". Applicant respectfully submits that the Hatano et al. publication as relied upon by the Examiner does not disclose these features, and that claims 23-25 therefore distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least these reasons.

Conclusion

As noted above, Applicant respectfully submits that the finality of the current Office Action dated November 26, 2003, is clearly improper. Accordingly, Applicant respectfully requests the Examiner to withdraw the finality of the current Office Action dated November 26, 2003, and to enter the above noted amendments.

Applicant further respectfully submits that the claims have been currently amended merely to improve form, not to further distinguish over the relied upon prior art. Accordingly, the amendments should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870

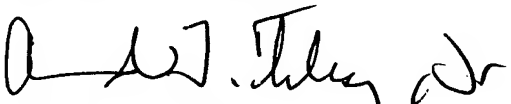
in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to March 26, 2004, for the period in which to file a response to the outstanding Office Action. The required fee of $110.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosures: Excerpt of Mead et al. textbook